REMARKS

In response to the Office Action dated 28 March 2000, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 1-16, 18-20, 28, 29, and 32-72 are pending in the application. Claims 1-6, 8-16, 19, 20, 28, 29, 32-37, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, 71, and 72 have been rejected. Claims 7, 18, 38-42, 44-48, 50, 52-54, 56, 58-60, 62, 64 and 66-70 have been objected to. Claims 29, 66, 68 and 70 have been amended, and new claims 73-78 have been added. No new matter has been added.

Information Disclosure Statements

In the Final Office Action dated 15 March 1999 the Examiner indicated that a legible copy of Suzaki et al. was not provided with the Information Disclosure Statement filed on March 19, 1998. Accordingly, the applicant has resubmitted Suzaki et al. on the 1449 herewith. The applicant respectfully requests that Suzaki et al. be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicants further request that a copy of the enclosed form 1449 be initialed by the Examiner and returned with the next official communication.

Allowable Subject Matter

The Examiner indicated that the subject matter recited in claims 7, 18, 38-42, 44-48, 50, 52-54, 56, 58-60, 62, 64 and 66-70 is allowable.

Objection

Claim 29 was objected to, and has been amended to obviate the objection.

Rejection Under 35 U.S.C. § 112

Claims 19, 28, 29, 32, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61, 63, 65, 67, 69, and 72 were rejected under 35 U.S.C. § 112, second paragraph. The applicant respectfully traverses.

The Examiner objected to the limitation: "the intergate dielectric has a permittivity that is higher than a permittivity of silicon dioxide."

Support for this limitation is found in the specification as the Examiner has indicated. The applicant respectfully submits that permittivity is a property of each material or substance, and is known to those skilled in the art. Therefore, a limitation drawn to the permittivity of the intergate dielectric clearly indicates to one skilled in the art the limits of the claimed invention.

Rejection Under 35 U.S.C. § 102

Claims 1-6, 8, 9 and 29 were rejected under 35 U.S.C. § 102(b) in view of Sakata et al. (Electronics Letters, Vol. 30, No. 9, pp.688-689, Sakata). The applicant respectfully traverses.

Claim 29 recites a memory cell comprising, among other elements, a storage electrode to store charge, and a control electrode separated from the storage electrode by an intergate dielectric.

Sakata does not disclose an electrode. Sakata discloses in Figure 1 a heterojunction comprising c-Si, a layer of hydrogenated amorphous silicon carbide (a-SiC:H), a layer of hydrogenated amorphous silicon (a-Si:H), another layer of a-SiC:H, and Al. Column 3. Both a-SiC:H and a-Si:H are highly resistive, insulating layers. Both are hydrogenated to ensure high resistivity. A plot of capacitance-voltage (C-V) characteristics for the heterojunction is shown in Fig. 2 of Sakata. The plot shows that the "capacitance at 3V (470pF) is in fairly good agreement with the calculated capacitance of stacked insulator layers." Column 2.

An electrode is known to those skilled in the art as a continuous, electrically conductive structure. For example, a floating gate is disclosed in the description as comprising polysilicon (page 16, line 3) or silicon carbide (page 11, line 17) according to embodiments of the invention. Sakata is disclosing a heterojunction comprised entirely of "stacked insulator layers", and does not disclose a continuous, electrically conductive structure.

Sakata discloses that both electrons and holes "can be stored in the a-Si:H layer because of the discontinuity of the conduction (valence) band edges at the a-SiC:H/a-Si:H interfaces." Column 1. However, Sakata has not substantially identified the mechanism for the charge storage: "We speculate that traps in the a-Si:H and/or at the interface between a-Si:H and a-SiC:H are acting as memory sites." Column 2. The band edges shown in Figure 1 are also pure

speculation by Sakata: "However, we speculate that a band offset exists at both band edges in the present samples, as schematically shown in Fig. 1, because both electrons and holes are stored in the a-Si:H layer." Column 2. The storage mechanism in the heterojunction disclosed by Sakata is a product of pure speculation, and therefore Sakata does not disclose an electrode.

The C-V plot shows a "large hysteresis" that may be used as a memory window. Column 2. While the hysteresis may be used to create a memory device, this does not imply that the heterojunction has an electrode. The heterojunction of Sakata is comprised entirely of alternate layers of highly resistive insulators, and does not include an electrode.

The applicant respectfully submits that Sakata does not disclose all the elements recited in claim 29, such as the storage electrode, that claim 29 is not anticipated by Sakata, and that claim 29 is in condition for allowance. Claims 1-6, 8, and 9 are dependent on claim 29. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 1-6, 8, and 9 are not anticipated by Sakata, and that claims 1-6, 8, and 9 are in condition for allowance.

Rejection Under 35 U.S.C. § 103

Claims 10-16, 20, 28, 32-37, 43, 49, 51, 55, 57, 61, 63, 65, 71 and 72 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakata in view of Sugita (JP Application No. 08-255878). The applicant respectfully traverses.

Claim 28 recites a transistor comprising, among other elements, a source region, a drain region, a channel region between the source region and the drain region, and a floating gate separated from the channel region by an insulator.

Sakata is deficient in the following manner. As described above, Sakata discloses a heterojunction structure that does not include an electrode or a floating gate. Sakata also does not include a source region or a drain region.

Sugita discloses a traditional floating gate transistor with a source, a drain, and a polysilicon floating gate. However, there is no suggestion to combine Sakata and Sugita. There must be a showing of a "teaching or motivation to combine prior art references" to support a rejection under section 103 and "the showing must be clear and particular." *In re Dembiczak,* 50 USPQ2d 1614, 1617 (Fed. Cir. 1999). Such a showing of a "teaching or motivation to combine"

is necessary to avoid the use of hindsight when combining references under section 103. 50 USPQ2d at 1616-17.

The heterojunction structure disclosed by Sakata operates in a manner very different from the operation of the floating gate transistor of Sugita. In fact, Sakata has only speculated on the reasons for the performance of the heterojunction. The operation of a traditional floating gate transistor is well known. The heterojunction is not similar to a transistor, and operates without a source region or a drain region. Neither Sugita nor Sakata would be improved by an addition from the other. Therefore there is no suggestion in either Sakata or Sugita for combining the two different structures.

The applicant respectfully submits that Sakata and Sugita do not disclose or suggest all the elements recited in claim 28, and that claim 28 is in condition for allowance. Claims 11-16 and 20 are dependent on claim 28. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 11-16 and 20 are not disclosed or suggested by Sakata and Sugita, and that claims 11-16 and 20 are in condition for allowance.

Claims 32-37, 43, 49, 51, 55, 57, 61, 63, 65, 71 and 72 recite elements similar to those recited in claim 28. For the reasons stated above, and the limitations in the claims, the applicant respectfully submits that claims 32-37, 43, 49, 51, 55, 57, 61, 63, 65, 71 and 72 are not disclosed or suggested by Sakata and Sugita, and that claims 32-37, 43, 49, 51, 55, 57, 61, 63, 65, 71 and 72 are in condition for allowance.

New Claims

The applicant has added new claims 73-78, and respectfully submits that they are in condition for allowance.

CONCLUSION

The applicant respectfully submits that all of the pending claims are in condition for allowance and such action is earnestly solicited. The Examiner is invited to telephone the below-signed attorney at 612-373-6973 to discuss any questions which may remain with respect

to the present application. If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 28 JUNE 2000

By _____
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Assistant Commissioner of Patents, Washington, D.C. 20231 on June 28 2000.

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Name

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Signature